General Remarks:

Office Action B included claim rejections and objections in two categories.

In Office Action B, Amendment A claim **9** was rejected and clarification of Amendment A claim **10** was requested under 35 U.S.C. 112, second paragraph. Both original claims were allowed in Office Action A pending re-writing in independent form, as their parent claim original claim **1** was rejected in Office Action A and cancelled in Amendment A. In this Amendment B, Applicant has attempted to correctly re-write claim **9** so that both claim **9** and dependent claim **10** are acceptable. Discussion of the revisions and support from the original Specification are presented below.

Amendment A claims **2** and **7-11** were rejected in Office Action B under 35 U.S.C. 103(a) as unpatentable over O'Shaughnessy (US 6,166,670) in view of Panicacci et al (US 6,885,396). Rejection of claim **2** also resulted in objections to dependent claims **3-6**. Applicant finds multiple deficiencies in Office Action B analysis of O'Shaughnessy, including failure to identify basic circuit components, connectivity and function. Further, discussion of Panicacci et al in Office Action B is limited to broad generalities without any specific technical discussion. Applicant's detailed objections are presented at length and in detail below. Applicant contends that Office Action B failed to demonstrate suggestion or motivation for the proposed combination, that the proposed combination fails to have a reasonable expectation of success, that the component parts in the combination no longer perform their intended function, and that the proposed combination fails to teach or suggest all the claim limitations of any of the claims rejected under 35 USC 103(a). Applicant therefore requests withdrawal of all 35 U.S.C. 103(a) rejections and objections of Office Action B.

Applicant notes an August 26, 2005 telephone call to examiner requesting clarification of Office Action B discussion of O'Shaughnessy in view of Panicacci. Examiner did not have Application immediately on hand and suggested that Applicant put any comments in writing in the subsequent Amendment (i.e. this Amendment B).

Claim rejections – 35 U.S.C 112

Office Action B rejected Amendment A claim **9** under 35 U.S.C. 112, second paragraph, and requested clarification of Amendment A claim **10**. Both claims as originally drafted in the original Application were allowed in Office Action A pending re-writing in independent form with all the limitations of their original parent claim **1** from the original Application.

Applicant appreciates Office Action B notification that the revised versions of the claims proposed by Applicant in Amendment A were not adequate. With this Amendment B, Applicant has attempted to re-write the claims to meet the requirements for allowance laid out in Office Action A and to avoid the 35 U.S.C. 112, second paragraph grounds for rejection in Office Action B.

Specifically, in claim **9**, Applicant has separated the limitation of original claim **9** from the limitations of original parent claim **1**. In Amendment A claim **9**, these limitations were combined as item b parts i-iv. Item b parts i-iii were from original parent claim **1**, while item b part iv was from original claim **9**. With this Amendment B, item b part iv becomes item d.

This change clarifies that in claim **9**, the digital logic gate element is not necessarily a separate and distinct element from the first transistor and the second transistor. The change also clarifies claim **10**, which narrows claim **9** by requiring that the digital logic gate comprise the two transistors. In other words, in Amendment B claim **9**, the threshold detector comprises the first transistor and the second transistor, and the threshold detector comprises the digital logic gate. In claim **10**, the threshold detector comprises the digital logic gate, and the digital logic gate comprises the first transistor and the second transistor.

Support in the figures

Figure 1A clearly depicts all of the elements of this Amendment B claim **9** as intended in original claim **9** and in Amendment A claim **9**, except for the first transistor and second transistor. There is a first sensor having a first sensor output – namely photodiode **10** –

connected to an inverter **20** with a digital inverter output **22**. Succeeding Fig. 1B replaces the schematic symbol of inverter **20** with a CMOS inverter composed of a p-type transistor **24** and an n-type transistor **26** whose gates are both connected by a wire to the output of photodiode **10**. The caption of Fig. 1A from page 7 of the specification is "Figure 1A shows a pinned photodiode driving an inverter". The caption of Fig. 1B is "Figure 1B shows a pinned photodiode driving an inverter composed of two MOSFETS". An inverter is a digital logic gate well known in the prior art.

Support in the specification

Applicant included numerous supporting statements for the inventions of claims **9** and **10** in the original specification.

In the OBJECTS AND OBJECTIVES SECTION on page 6 lines 9-13, original specification reads:

> It is another object of the present invention to demonstrate that CMOS logic gates with minimum-size transistors are suitable as local threshold detectors, resulting in area-efficient sensor cells.
>
> It is a further object of the present invention to show that a CMOS inverter is a very efficient circuit for threshold detection.

Later, in the section DESCRIPTION – ALTERNATIVE EMBODIMENTS WITH MINIMUM TRANSISTOR SIZES on pages 10 and 11, there is extensive discussion of digital logic switching characteristics relative to transistor sizing.

Immediately after this, there is a section on pages 11 and 12 entitled DESCRIPTION – ALTERNATIVE EMBODIMENTS WITH OTHER PRIOR ART DIGITAL LOGIC CIRCUITS which reads as follows:

> Inverters are not the only digital logic gates suitable for the present invention, though they are the smallest and least-complicated. There are many different types of digital logic gates that can be used in the present invention, such as

AND, OR, NAND, NOR, XOR, and other gates. Many of these gates have more than one input, often two in their simplest forms.

A two-input digital logic gate would be useful in synchronizing operation of the threshold detector. For instance, a 2-input AND gate could have as one input a sensor output and as the other input a control signal indicating when the detector should operate. The AND gate output would switch only with the control signal in a logic 1 state and given a suitable sensor output change.

Logic gates can also be used to emulate other logic gates, particularly in technologies such as field programmable gate arrays. For instance, applying the same signal to both inputs of a 2-input NAND gate produces the same digital input-output response as an inverter.

With respect to the three paragraphs quoted in full just above, the first paragraph clearly describes Applicant's idea that inverters are not the only digital logic gates which can be used as threshold detectors in the invention, in particular threshold detectors with one analog input (the sensor output) and an implicit threshold level.

The second paragraph further describes use of a 2-input AND gate – which is not an inverter – as a threshold detector in the present invention. The idea presented is to have a digital enable signal applied to one input of the 2-input AND gate, and the analog sensor output applied to the other. When the enable signal is low, the threshold detector is effectively off. When the enable signal is high, the threshold detector's digital output depends on the analog sensor output passed to the second gate input.

Even though original Application did not include a figure specifically depicting the material in the second paragraph cited above, Applicant submits that the function and construction of a 2-input AND gate is well known in the prior art. Based on Applicant's text description, an individual skilled in the prior art would immediately recognize the analogous function of this device to the inverters depicted in Applicant's figures and how to place them in the present invention.

Moreover, it is well known that an easy and efficient way to create a 2-input AND gate is to invert the output of a 2-input NAND gate, complementary logic (such as a NAND gate) being a natural result of n-type transistors pulling low when their inputs are high and p-type transistors pulling high when their inputs are low. The paragraph therefore suggests claim **9** in which the threshold detector includes a first transistor and second transistor (pull-up and pull-down transistors with gates connected together to form the NAND gate input which receives the analog sensor output) and a digital logic gate (the inverter which inverts the NAND output to provide the AND output).

It is understood in the prior art that an inverter is a digital logic gate. It is also understood in the prior art that a 2-input AND gate is a digital logic gate. The second quoted paragraph therefore also suggests claim **10**, in which the threshold detector comprises a digital logic gate (the 2-input AND gate) which comprises the first transistor and the second transistor (pull-up and pull-down transistors with gates connected together to form the AND gate input which receives the analog sensor output).

The third quoted paragraph clearly identifies how to used a 2-input NAND gate to mimic the performance of an inverter. Successful use of this in the invention is again obvious to one skilled in the prior art. In this case, the threshold detector comprises a digital logic gate – the 2-input NAND with its inputs connected together – which in turn comprises the first transistor and the second transistor with gates connected to the analog sensor output, as well as two other similarly-connected transistors. The paragraph thus clearly describes claim **10**.

With respect to the second quoted paragraph, it is accepted in the prior art that digital logic gates can be composed of sets of non-digital-logic-gate transistors (e.g. an inverter made of a pull-up p-type transistor and an n-type pull-down transistor) or of combinations of other digital logic gates (e.g. a 2-input AND gate made of a 2-input NAND gate followed by an inverter), or both. Different interpretations of a single element – identical circuits as "a 2-input AND gate" and "a 2-input NAND gate followed by an inverter", for instance – are common in the prior art and well understood. However, the Office Action B assertion that claim **9** is indefinite and therefore rejected under 35 USC 112 second paragraph seems to be based, according to the discussion of Office Action B page 2, of a preferred interpretation of claim **9** having separate transistors and digital

logic gate. Applicant notes that MPEP 2173.02 indicates that an examiner "should not reject claims or insist on their own preferences if other modes of expression selected by applicants satisfy the statutory requirements" and further that MPEP 2173.04 indicates that "breadth is not indefiniteness". Also, MPEP 2173.06 requires that claims be "given the broadest reasonable interpretation consistent with the specification".

In light of common practice in the prior art, Applicant submits that it is reasonable for claim **9** to include a threshold detector comprising the first transistor, the second transistor, and the digital logic gate without the specific interpretation that the digital logic gate does not comprise the two transistors, and for dependent claim **9** to narrow the scope with the requirement that the digital logic gate does comprise the two transistors. Claim **9** admits a broad interpretation, but it does "set out and describe a particular area with a reasonable degree of precision and particularity". In other words, claim **9** answers the essential question of 35 U.S.C. 112 second paragraph.

Summary of 35 U.S.C. 112 rejection discussion

Applicant submits that both claim **9** and claim **10** are well-supported in the specification such that a figure is not necessary for a skilled practitioner to be able to implement a working version of the invention as defined by the claims. The function and use of the most-efficient digital logic gate for the implicit-threshold threshold detector – namely a CMOS inverter – was described in detail in prose and in figures. Subsequently, use of other digital logic gates in an analogous fashion was discussed. Specific non-inverter digital logic gates were presented. The function and construction of these gates were presumed within the knowledge of a skilled practitioner.

Applicant has re-written Amendment A claim **9** to more closely match previously allowed original claim **9**.

Applicant therefore submits that Amendment B claim **9** is in fact clearly defined and discussed in the specification such that a practitioner of the art could make the invention according to claim **9**. Applicant therefore requests withdrawal of the 35 USC 112 second paragraph rejection of claim **9**. Applicant has also clarified claim **10** and submits that it too is in allowable condition.

Claim rejections – 35 U.S.C. 103

Office Action B rejected Amendment A claims **2** and **7-11** under 35 U.S.C. 103(a) as "being unpatentable over O'Shaughnessy (US 6,166,670) in view of Panicacci et al (US 6,885,396)."

Office Action B support for this consists of paragraphs 2 and 3 from page 3, quoted in their entirety below:

> O'Shaughnessy teaches in figure (10) a digital-to-analog converter comprising: a first inverter functioning as a threshold detector that must have a given threshold level, the inverter including an NMOS transistor (1084) having a first gate, a PMOS transistor (1091) having a second gate, the transistors joined at their drains to form the first inverter (See Column 15, lines 9-12), both transistors receiving at their respective gate an analog input signal (AVDD); a second inverter/logic gate (1021).
>
> O'Shaughnessy does not specifically teach a sensor circuit whose output is the analog signal applied to the transistors. However, the use of a sensor circuit is an imaging system is well known in the art, as evidenced by Panicacci et al. Panicacci et al teach an analog-to-digital conversion apparatus for an image sensor wherein an analog input signal is sensed by a sensor and fed to the remainder of the circuit for further processing. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Panicacci et al and O'Shaughnessy to build an imaging system having improved performance and reliability because that would increase the overall speed and accuracy of the output stage (See column 1, lines 47-49).

Applicant will show the following with respect to O'Shaughnessy:

- 1 – O'Shaughnessy figure 10 does not teach a digital-to-analog converter, but rather a charge pump for calibrating current sources in a particular type of digital-to-analog converter.
- 2 – NMOS transistor 1084 does not receive AVDD at its gate.

- 3 – PMOS transistor 1091 does not receive AVDD at its gate.
- 4 – There is no signal in O'Shaughnessy figure 10 received at the gates of both NMOS transistor 1084 and PMOS transistor 1091.
- 5 – AVDD is not an analog input signal, but rather a positive power supply for the analog portion of the circuitry in O'Shaughnessy figure 10.
- 6 – The inverter formed by NMOS transistor 1084 and PMOS transistor 1091 does not function as a threshold detector, but rather as an amplifier to boost the input-referred capacitance at the OUT node.

Applicant will show the following with respect to the combination proposed in Office Action B:

- 7 – The combination of O'Shaughnessy and Panicacci et al implied in the first sentence of paragraph 3 suggests a circuit so unusual as to itself be patentable if technically feasible.
- 8 – The subsequent comments in paragraph 3 about the contents of Panicacci et al are broadly obvious and do not point out with any specificity any connections to the present invention.
- 9 – The concluding statement of motivation for the combination misinterprets the material discussion in Panicacci et al directly, and from a basic engineering design perspective is incorrect.

Applicant will further submit that the combination fails to include all of the limitations of any of the rejected claims, is unlikely to produce the results claimed by the motivation statement in Office Action B page 3 paragraph 3, and that the components of the combination no longer perform their original functions.

1 – O'Shaughnessy figure 10 does not teach a digital-to-analog converter, but rather a charge pump for calibrating current sources in a particular type of digital-to-analog converter

Office Action B states in paragraph 2 on page 3 that "O'Shaughnessy teaches in figure (10) a digital-to-analog converter".

The title of O'Shaughnessy is SELF-CALIBRATING CURRENT MIRROR AND DIGITAL-TO-ANALOG CONVERTER. The caption given in the O'Shaughnessy specification for Fig. 10 is the following, from Column 7, lines 26-28:

> Fig. 10 is a schematic of a charge pump circuit that utilizes "Miller Effect" to reduce the step size of the output voltage of the charge pump.

On Column 14, lines 55-58, O'Shaughnessy states:

> FIG. 10 discloses the schematic of a charge pump circuit having a reduced step size output voltage. The reduced step size is obtained using Miller feedback capacitance and by using a restricted pump input voltage.

O'Shaughnessy states on Column 15, lines 55-63:

> The purpose of the charge pump in the various embodiments of the self-calibrating current mirrors is to provide an incremental voltage step to the gate of a current mirror MOS transistor. The smaller the voltage step, the more precise [SIC] the current mirror output current will replicate the input current. The charge pump of FIG. 10 uses Miller feedback capacitance and a restricted voltage range to provide a reduced voltage step. The charge pump of FIG. 10 is extremely well suited as a charge pump in a self-calibrating current mirror.

The circuit of Fig. 10, exclusive of PMOS transistor **1010**, is a charge pump. Its main purpose is to regulate the voltage at the output node OUT **1090** which is applied to the gate of PMOS transistor **1010**, which is acting as a current source. The regulation consists of transferring charge on to or off of holding capacitor **1094** through transfer

gate **1023**, and then storing or removing charge at output node OUT **1090** via transfer gate **1024**.

The circuit in Fig. 10 has digital control signals and an analog output signal, but is not itself a digital-to-analog converter. At best, Fig. 10 depicts a component part which is useful in improving the performance of, but which is not vital to, a switched-current digital-to-analog converter.

Note also that in the Application, there are no occurrences of any of the following common digital-to-analog conversion terms – "DAC", "D/A", "D/A converter", or "digital-to-analog". In contrast, in O'Shaughnessy, there are no occurrences of any of the following common analog-to-digital conversion terms – "ADC", "A/D", "A/D converter", or "analog-to-digital".

2 – NMOS transistor 1084 does not receive AVDD at its gate

Office Action B indicates in paragraph 2 on page 3 that NMOS transistor **1084** receives at its gate an analog input signal AVDD.

Referring to O'Shaughnessy Fig. 10, NMOS transistor **1084** receives at its gate the output from BIAS CIRCUIT **1080**. This signal is clearly not AVDD. If it were, the implication would be that NMOS transistor **1084**, NMOS transistor **1082**, and NMOS transistor **1081** were all tied to AVDD, and there would be no need of a separate BIAS CIRCUIT **1080**.

While O'Shaughnessy does not discuss the details of BIAS CIRCUIT **1080** explicitly, the purpose of biasing circuits is well understood in the prior art of analog circuit design. Biasing of NMOS transistor **1084** will be further discussed below, with regard to point 5.

3 – PMOS transistor 1091 does not receive AVDD at its gate

Office Action B indicates in paragraph 2 on page 3 that PMOS transistor **1091** receives analog input signal AVDD at its gate.

Referring to O'Shaughnessy Fig. 10, PMOS transistor **1091** has its source connected to AVDD. The gate of PMOS transistor **1091** is connected to the output node OUT **1090**. This node is connected to the gate of the current source PMOS transistor **1010**, to the feedback capacitor **1092**, to the source of a pre-charge PMOS transistor **1094**, and to transfer gate **1024**.

The voltage at output node OUT **1090** can never reach the voltage at AVDD. When pre-charge PMOS transistor is turned on, PMOS transistor **1091** is connected in a diode configuration and the drain voltage cannot rise above a diode drop below AVDD. Similarly, since PMOS transistor **1011** is permanently connected in a diode configuration, the voltage on holding capacitor **1094** is restricted to a diode drop below AVDD when transfer gate **1023** is on. When transfer gate **1023** is off and transfer gate 1024 is on, holding capacitor **1094** is connected to the gate of PMOS transistor **1091**, but there is no way to transfer all the charge from holding capacitor **1094** to feedback capacitor **1092**.

4 – There is no signal in O'Shaughnessy figure 10 received at the gates of both NMOS transistor 1084 and PMOS transistor 1091

Office Action B in paragraph 2 on page 3 states that "both transistors [receive] at their respective gate an analog input signal (AVDD)"

In fact, on inspection of O'Shaughnessy Fig. 10, not only is AVDD not applied to both gates, there is no signal which is applied to both gates.

5 – AVDD is not an analog input signal, but rather a positive power supply for the analog portion of the circuitry in O'Shaughnessy figure 10

Office Action B in paragraph 2 on page 3 indicates that "AVDD" is "an analog input signal".

In O'Shaughnessy Fig. 10, AVDD actually indicates a positive power supply rail, not an analog input signal. In mixed-signal circuits, it is common practice to supply analog and digital circuitry with separate power supply rails. Large numbers of digital circuits

switching simultaneously can cause power supply spikes or droops which are not a problem for digital circuits but which are a problem for analog circuits. Hence, a "dirty" power supply may be provided for digital circuits, while a "clean" power supply is provided for analog circuits. Typically, analog and digital positive power supply rails may be differentiated as "AVDD" and "DVDD". Similarly, there may be separate analog and digital ground power supply rails.

Considering O'Shaughnessy Fig. 10, AVDD is connected to the source of PMOS transistor **1091**, not to the gate. While AVDD is connected to one terminal of holding capacitor **1094**, this does not mean it is connected to the gate of PMOS transistor **1091**. Ideally, the power supply voltages are constant, so holding capacitor **1094** represents an open circuit, not a connection. Assertion otherwise, clearly implied by Office Action B, is too broad an interpretation of connectivity. In an actual implementation, parasitic capacitors exist between every realized element of Fig. 10 and every other element – and in fact, between every realized element of Fig. 10 and a rock on the other side of the moon. Philosophically, there is universal connectivity, but one skilled in the art will recognize that a practical definition is necessarily much narrower.

6 – The inverter formed by NMOS transistor 1084 and PMOS transistor 1091 does not function as a threshold detector, but rather as an amplifier to boost the input-referred capacitance at the OUT node

Office Action B states in paragraph 2 on page 3 that Fig. 10 comprises "a first inverter functioning as a threshold detector that must have a given threshold detector", the first inverter being composed of NMOS transistor **1084** and PMOS transistor **1091**. The only support for this in Office Action B is the following reference from O'Shaughnessy, Column 15, lines 9-12:

> The drain of PMOS transistor 1091 is connected to the drain of the third NMOS transistor 1084 to form an inverter.

An actual examination of Fig. 10 reveals that NMOS transistor **1084** and PMOS transistor **1091** do not function as a threshold detector.

A more appropriate description than "inverter", with its connotations of digital logic gates, is that the transistors form an "inverting amplifier". This inverting amplifier has a small-signal negative gain from input to output which is determined by the slope of the DC transfer function at the output bias point. Call this gain "-G". Feedback capacitor **1092** is connected across the inverting amplifier. Call its nominal capacitance "C". In this configuration, the input-referenced capacitance is (1 + G)*C because of the Miller Effect.

In other words, the purpose of PMOS transistor **1091** and NMOS transistor **1084** is to amplify the capacitance at the output node OUT **1090** as seen by the output of transfer gate **1024**. For useful amplification, BIAS CIRCUIT **1080** must supply a gate input to NMOS transistor **1084** that biases the inverting amplifier output in the transition region between the power supply rails where the transfer function has a steep slope. Ergo BIAS CIRCUIT **1080** is not supplying the gate of NMOS transistor **1084** with a signal having the same value as AVDD.

The main advantage of this active Miller Effect capacitance amplifier is that in an integrated circuit implementation, the feedback capacitor and the two transistors forming the negative gain (i.e. inverting) amplifier have a much smaller footprint than would a capacitor with a (1 + G)*C nominal value.

Summary of Office Action B discussion of O'Shaughnessy

Applicant therefore submits the following with respect to O'Shaughnessy:

- On its own, O'Shaughnessy does not motivate or suggest analog-to-digital conversion.
- On its own, O'Shaughnessy lacks the following limitations of Amendment A claim **2**:
    - a first sensor having a first sensor output
    - a threshold detector with a first analog input having the first sensor output applied as the first analog input
    - in the threshold detector, means for applying the first analog input to the gate of a first transistor which is an n-type MOS transistor

- in the threshold detector, means for applying the first analog input to the gates of both the first transistor and a second transistor
- in the threshold detector, the second transistor being a p-type MOS transistor

- On its own, O'Shaughnessy lacks the following limitations of Amendment A claim **7**:
  - a first sensor having a first sensor output
  - a threshold detector with a first analog input having the first sensor output applied as the first analog input
  - in the threshold detector, means for applying the first analog input to the gates of both a first transistor and a second transistor
  - the threshold detector comprising an inverter
- On its own, O'Shaughnessy lacks the following limitations of Amendment A claim **8**:
  - the recited missing limitations of parent Amendment A claim **7**, and
  - the inverter comprising the first transistor and the second transistor
- On its own, O'Shaughnessy lacks the following limitations of Amendment A claim **9**:
  - a first sensor having a first sensor output
  - a threshold detector with a first analog input having the first sensor output applied as the first analog input
  - in the threshold detector, means for applying the first analog input to the gates of both a first transistor and a second transistor
  - the threshold detector comprising a digital logic gate
- On its own, O'Shaughnessy lacks the following limitations of Amendment A claim **10**:
  - the recited missing limitations of parent Amendment A claim **9**, and
  - the digital logic gate comprising the first transistor and the second transistor
- On its own, O'Shaughnessy lacks the following limitations of Amendment A claim **11**:
  - a first sensor having a first sensor output
  - a threshold detector with a first analog input having the first sensor output applied as the first analog input

- in the threshold detector, means for applying the first analog input to the gate of a first transistor which is an n-type MOS transistor
- in the threshold detector, means for applying the first analog input to the gates of both the first transistor and a second transistor
- in the threshold detector, the second transistor being a p-type MOS transistor
- that the threshold detector is a single-input threshold detector with an implicit threshold level

7 – The combination of O'Shaughnessy and Panicacci et al implied in the first sentence of paragraph 3 suggests a circuit so unusual as to itself be patentable if technically feasible

Office Action B paragraph 3 on page 3 begins with the following statement connecting O'Shaughnessy and Panicacci et al:

> O'Shaughnessy does not specifically teach a sensor circuit whose output is the analog signal applied to the transistors.

Based on the Office Action B discussion of O'Shaughnessy on the immediately preceding paragraph 2 of page 3, Office Action B's suggested combination is a sensor output applied to Fig. 10 as AVDD. In Fig. 10, AVDD is supplied to the source of transistor **1011**, to one terminal of holding capacitor **1094**, to the source of transistor **1094**, and to the source of transistor **1010**.

In other words, the combination of O'Shaughnessy and Panicacci et al. suggested by Office Action B is a sensor whose output directly powers analog circuitry for a charge pump which is used to calibrate a current source in a steered-current digital-to-analog converter – and which also provides the current for the source being calibrated!

Applicant concedes that there are research efforts underway which are aimed at developing self-powered circuits, for instance, MEMS devices whose mechanical vibrations are converted to electrical energy which is stored and used to power other circuits. However, the combination of O'Shaughnessy and Panicacci et al suggested in

Office Action B page 3 paragraph 3 does not make sense given the vast body of prior art. Sensor outputs are weak signals which are amplified and processed with follow-on circuitry, not signals which power such circuitry. Office Action B's combination is so unusual that if it were technically feasible – which is by no means obvious or certain – it would be patentable.

Applicant submits that the combination of O'Shaughnessy and Panicacci et al recited in Office Action B does not have a reasonable expectation of success. Moreover, by applying a sensor output directly to the charge pumps and current mirrors in a steered-current digital-to-analog converter, that converter no longer performs its function, which is to take known digital number representations (binary strings, typically) as inputs and map them to quantized analog signal values as output. If the positive analog power supply rail AVDD varies significantly, then the sourced currents will vary significantly as well even if for some reason the sensor can supply the currents. The quantized analog signal value output then depends on both the known digital number representation inputs and on the variable value of AVDD. Even if the charge pumps and the current sources still function, the digital-to-analog converter of which they are components provides a random and ambiguous analog output mapping. The mapping is random because the sensor output is unknown; and ambiguous because the range of output voltages for two different known digital number representation inputs could overlap depending on level of the sensor output provided as AVDD. The converter may well have differential and integral nonlinearity which are full range, rather than the sub-LSB amounts enabled by O'Shaughnessy's calibration circuits in the first place.

8 – The subsequent comments about the contents of Panicacci et al are broadly obvious and do not point out with any specificity any connections to the present invention

Office Action B paragraph 3 on page 3 continues:

> However, the use of a sensor circuit in an imaging system is well known in the art, as evidenced by Panicacci et al. Panicacci et al teach an analog-to-digital conversion apparatus for an image sensor wherein an analog input signal is sense by a sensor and fed to the remainder of the circuit for further processing.

With respect to these statements, every electronic imaging system has some form of sensor circuit and some form of additional processing. These statements do not explain any of the details of Panicacci et al or of the present invention or how one relates to the other. They also do not clarify the combination of Panicacci et al and O'Shaughnessy proposed by Office Action B.

9 – The concluding statement of motivation for the combination misinterprets the material discussion in Panicacci et al directly, and from a basic engineering design perspective is incorrect

Office Action B paragraph 3 on page 3 concludes with the following statement:

> It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Panicacci et al and O'Shaughnessy to build an imaging system having improved performance and reliability because that would increase the overall speed and accuracy of the output stage (See column 1, lines 47-49).

Panicacci et al Column 1 lines 47-49 state:

> Recently there has been heightened interest in parallel column architectures to increase the overall speed and/or accuracy of the output stage.

In the context of CMOS imaging systems, Panicacci et al's statement is quite general. The "heightened interest" reflects the fact that single-chip CMOS imaging arrays have been getting quite large in sensor count – up to 14.4 million pixels in commercially available products at the time of writing. Latency time for video applications is 1/30 of a second or less, but even for digital still photography long latency times – say, more than a half-second – are unacceptable. Required raw throughput is very high. Parallel column architectures allow processing of multiple sensor outputs simultaneously at slower speeds and higher resolutions than would be required with serial processing.

In the realm of A/D converters, there is not a constant cost-for-performance envelope. For instance, suppose a 10 megapixel CMOS imager must have a 0.1 second latency time at 12 bits per pixel. With purely serial A/D conversion, a single 12-bit, 100M sample/second A/D converter would be necessary to meet the specifications. However, such a converter might be bulky, power-hungry, and maybe even technically infeasible. On the other hand, 50 parallel 12-bit, 2M sample/second A/D converters could also be used to meet the specifications. They might be smaller, less power-hungry, and technically feasible where a single ultra-high-speed converter is not.

In the paragraph of Column 1 containing lines 47-49, Panicacci et al are discussing improvement of "overall speed and/or accuracy" by division of labor. Multiple elements with modest capabilities can do the same job as one element with extraordinary capabilities, and – importantly – at a lower cost.

Redux of basic engineering design principles

Office Action B page 3 paragraph 3 concludes with a statement which implies that there is a causal monotonic relationship between "performance and reliability" and "overall speed and accuracy". The implication is that "improved performance and reliability...would increase the overall speed and accuracy of the output stage". In other words, better "performance and reliability" results in increased "overall speed and accuracy". This is incorrect.

Improved performance and reliability do not necessarily result in increased speed and accuracy, and increased speed and accuracy do not necessarily result in improved performance and reliability. It is true that in some systems, speed and accuracy are measures of performance, but there are other measures as well.

As an example, consider an imaging system being designed for a deep space environment – say for an orbiting satellite or an interplanetary probe – on a strict budget of consumed power and system size.

Running the circuits of the imaging system as fast as possible might be a waste of power that could be used for some other part of the overall system – control, communications,

propulsion, et cetera. Also, aiming for the maximum possible speed may add considerable effort and cost to the design cycle because of stringent timing requirements, possibly limiting chip space and design resources that could be allocated to other critical features. Thus, increasing overall speed can lead to decreases in performance and reliability.

Adding circuitry to improve A/D conversion might require using less-robust radiation-hardening measures in order to meet the system size constraint. The system is then more accurate, but less reliable when deployed in the intended space environment where there are heavy amounts of ionizing radiation.

In the example, performance is not measured by speed and accuracy alone. There are other performance measures, and design trade-offs among them. The best design might well be an imaging system that operates as fast as necessary – but no faster – with circuits that are as small as necessary – but no smaller.

Deficiencies of Office Action B combination of O'Shaughnessy and Panicacci et al.

Applicant therefore submits the following with respect to Office Action B's suggested combination of O'Shaughnessy and Panicacci et al:

- The combination lacks the following limitations of Amendment A claim **2**:
    - a threshold detector with a first analog input having a first sensor output applied as the first analog input
    - in the threshold detector, means for applying the first analog input to the gate of a first transistor which is an n-type MOS transistor
    - in the threshold detector, means for applying the first analog input to the gates of both the first transistor and a second transistor
    - in the threshold detector, the second transistor being a p-type MOS transistor
- The combination lacks the following limitations of Amendment A claim **7**:
    - a threshold detector with a first analog input having the first sensor output applied as the first analog input

- in the threshold detector, means for applying the first analog input to the gates of both a first transistor and a second transistor
- the threshold detector comprising an inverter

- The combination lacks the following limitations of Amendment A claim **8**:
  - the recited missing limitations of parent Amendment A claim **7**, and
  - the inverter comprising the first transistor and the second transistor
- The combination lacks the following limitations of Amendment A claim **9**:
  - a threshold detector with a first analog input having the first sensor output applied as the first analog input
  - in the threshold detector, means for applying the first analog input to the gates of both a first transistor and a second transistor
  - the threshold detector comprising a digital logic gate
- The combination lacks the following limitations of Amendment A claim **10**:
  - the recited missing limitations of parent Amendment A claim **9**, and
  - the digital logic gate comprising the first transistor and the second transistor
- The combination lacks the following limitations of Amendment A claim **11**:
  - a threshold detector with a first analog input having the first sensor output applied as the first analog input
  - in the threshold detector, means for applying the first analog input to the gate of a first transistor which is an n-type MOS transistor
  - in the threshold detector, means for applying the first analog input to the gates of both the first transistor and a second transistor
  - in the threshold detector, the second transistor being a p-type MOS transistor
  - that the threshold detector is a single-input threshold detector with an implicit threshold level

The only differences between O'Shaughnessy and the combination of O'Shaughnessy and Panicacci et al of Office Action B with respect to the limitations of the rejected claims of the Application are that the combination suggests analog-to-digital conversion in a CMOS imaging array and includes a first sensor having a first sensor output.

The Panicacci et al portion of the combination no longer has the same function as Panicacci et al on its own

Another problem with the combination is that the portion of it from Panicacci et al no longer functions. The suggestion is an analog sensor output supplied to O'Shaughnessy's charge pumps of Fig. 10 as AVDD. In Panicacci et al, the all the sensor outputs are locally amplified within APS cells. Referring to Panicacci et al Fig. 4A, the sensors are labeled photodiode **80**.

In the combination, once the first sensor is reset, charge is immediately drawn off to feed the analog circuits of O'Shaughnessy Fig. 10. But Panicacci et al has multiple sensors whose amplified outputs are multiplexed onto column buses. If only one of these sensors is providing current to a charge pump, it will have a completely different response than other sensors in the array. On the other hand, if more than one of these sensors provides AVDD, the drawn-off charge will depend on the individual sensor output levels, and again there will be a non-uniform response across the sensors in the array.

Even at the cell level (e.g. APS cells **50A** and **50B** in Panicacci et al Fig. 4A) where the cell outputs are amplified sensor outputs applied to a shared column bus, any current drawn from the column bus to power a charge pump of O'Shaughnessy et al Fig. 10 will distort the sampled-and-held signal at the S/H circuit **60A** or **60B** of Panicacci et al Fig. 4A.

Other reasons why the present invention is not suggested by O'Shaughnessy, Panicacci et al, or the combination of O'Shaughnessy and Panicacci et al

Aside from failing to have all the limitations of the present invention separately or in the suggested combination, the cited prior art of O'Shaughnessy and Panicacci et al teach art specifically contrary to that of the present invention, notably:

- 10 – O'Shaughnessy and Panicacci et al take entirely different approaches to performance improvement.

- 11 – Panicacci et al focus on a CMOS sensor structure which has a single-gate single-transistor amplifier.
- 12 – Subsequent sampling-and-holding and amplification in Panicacci et al have amplified analog signals applied to single transistor gates.
- 13 – Panicacci et al focus solely on a comparator with two explicit inputs.
- 14 – Panicacci et al's comparator is not acting as a threshold detector indicating when a changing analog signal reaches a given threshold.
- 15 – Panicacci et al's comparator output changes in response to changes in a generated known reference voltage.
- 16 – Overall speed in Panicacci et al arises from parallel use of relatively slow A/D converters, whereas speed in O'Shaughnessy is essentially serial.

10 – O'Shaughnessy and Panicacci et al take entirely different approaches to performance improvement

Relating the basic design principles discussed above to the cited prior art, O'Shaughnessy's material is aimed at providing a single low-resolution, high-speed D/A converter having low distortion. The distortion reduction is achieved using O'Shaughnessy's charge pump circuit to calibrate a set of nominally identical current sources. There is a charge pump circuit for each current source, and both grow exponentially in count with resolution. For the 10-bit D/A converter of O'Shaughnessy Fig. 11, there are (2^N – 1) = (2^10 – 1) = 1023 charge pump circuits and 1023 current sources.

In contrast, Panicacci et al's material is aimed at providing multiple low-speed A/D converters that in concert obtain high A/D throughput. Panicacci et al show an 8-bit successive approximation A/D converter in Fig. 11. This converter comprises 8 binary-scaled capacitors which can be switched between Vref1 and ground for generating sequences of known reference voltages, which are compared to an amplified, sampled-and-held, and further amplified sensor output to produce the desired digital number representation output.

O'Shaughnessy seeks to improve D/A converter performance by introducing a circuit to improve current source matching without reducing the converter speed. Panicacci et al seek to improve systemic A/D converter performance by allowing reduced speed for individual converters but maintaining throughput by using parallel converters each processing a pair of sensor array columns.

The two philosophies do not suggest that a high-speed low-distortion D/A converter yields better performance in a parallel low-speed multiplexed A/D converter. In fact, considering the reference generation section of Panicacci et al Fig. 4B, it's quite possible that 8 binary-scaled capacitors and some analog switches represent a much more desirable circuit than an O'Shaughnessy-based reference generator, which would have (2^8 – 1) = 255 charge pumps of Fig. 10 and ancillary circuitry of Fig. 11 plus some means for converting from an analog current to an analog voltage. This would be the case if the former system had a much smaller and power-efficient footprint. If, as would

be the case in an array with more than two columns, there are multiple instances of O'Shaughnessy-based reference generators, maintaining the low-distortion characteristics of O'Shaughnessy requires precise matching of whatever circuit elements are implementing the current-to-voltage conversion.

In contrast, in the present invention, performance improvement is obtained by taking the analog-to-digital conversion process right to the sensor by having its analog output applied as the input to a threshold detector immediately producing a digital output. The elaborate analog processing of amplification, transport out of array, sampling-and-holding, further amplification, analog reference generation, and comparison of Panicacci et al, and sharing of the circuits for these functions is avoided. Similarly, the elaborate circuitry for distortion reduction in O'Shaughnessy is avoided. Threshold detector matching does not matter provided the differential techniques of the Applicant's related application cited in the initial filing, now issued as US Patent 6,873,282.

11 – Panicacci et al focus on a CMOS sensor structure which has a single-gate single-transistor amplifier

In Panicacci's figures and text, the only CMOS sensor structure presented is an Active Pixel Sensor (APS) cell. As discussed in the Application, an APS cell consists of a reverse-biased photodiode as the sensor, an in-cell reset transistor, an in-cell amplifying transistor (hence "Active" in APS), and a bus access transistor. Right at the sensor – which is to say, at the photodiode – the sensor output is connected to exactly one transistor gate, which is the gate of the amplifying transistor. This is in stark contrast to the ideas of the present invention, where right at the sensor – at the photodiode – the sensor output is connected to at least two transistor gates as discussed in the Application's specification and claims.

To repeat some of the discussion in the Application, an APS cell is designed to have a small cell footprint. The single-transistor amplifier in a given cell drives a shared bus line that takes the amplified sensor output to processing circuitry located outside the array, including, in Panicacci et al, S/H, amplification, and A/D conversion circuitry. In the present invention, there is no single-transistor amplifier and there is no analog signal bus passing analog signals out of the imaging array. A/D conversion is accomplished with

the threshold detector having the sensor output as a direct analog input to a PMOS transistor gate and to an NMOS transistor gate and having a digital output indicating when that input causes a logic transition.

12 – Subsequent sampling-and-holding and amplification in Panicacci et al have amplified analog signals applied to single transistor gates

Considering the array-external processing in Panicacci et al's Figs. 4A and 4B, the sampled-and-held output from a given pixel is applied to the gate of a single transistor **M3** whose output drives one or more capacitors connected to the inverting input of op-amp **90**. **M3** is a single-transistor amplifier, and the front end of op-amp **90** is a differential pair. The output of amplification circuit **66** is further fed to another sample-and-hold circuit with a single-transistor amplifier **M7**.

At no point in this processing structure, and at no point in Panicacci et al's specification, is it suggested that a sensor signal, or even an amplified or otherwise processed sensor signal, be applied to the gates of two transistors, one an NMOS transistor and one a PMOS transistor.

13 – Panicacci et al focus solely on a comparator with two explicit inputs

The one element in Panicacci et al which suggests comparing one analog signal to another analog signal and indicating which is the greater is the unlabelled comparator providing **Vout** in Fig. 4B. One input of the comparator receives sampled-and-held output of op-amp **90**. The other input of the comparator receives the known generated signals produced by the successive-approximation ADC **52**.

This comparator has two explicit inputs. It is not an inverter or other digital logic gate. It does not have an implicit threshold. There is further nothing to suggest that either input is received by the gate of more than one transistor or by the gates of two different types of MOS transistors.

14 – Panicacci et al's comparator is not acting as a threshold detector indicating when a changing analog signal reaches a given threshold

With respect to the Application as a whole, the threshold detector discussed by the Applicant indicates when an unknown, time-varying input reaches a threshold. The threshold can be implicit and substantially constant from one conversion to another. Panicacci et al's comparator receives a sampled-and-held unknown analog input which is held fixed during one conversion cycle and compared to a discrete sequence of known generated reference voltages. It is possible for the output of the comparator to change states at each epoch of the successive approximation cycle. If the comparator is viewed as a threshold detector, the question arises of what is the threshold. In a given conversion cycle, the only constant input signal is the unknown input, in which case there isn't a constant threshold from conversion to conversion. On the other hand, if the unknown input is not the threshold, then there is no identifiable threshold because the other input changes at each stage of a single conversion cycle.

15 – Panicacci et al's comparator output changes in response to changes in a generated known reference voltage

The inputs to the comparator in Panicacci et al Fig. 4B are analog voltages defined by charge stored on capacitors. In contrast, the analog output of O'Shaughnessy's D/A converter is a current.

Using O'Shaughnessy's D/A converter to generate known reference signals in Panicacci et al – a combination not suggested in Office Action B – has clear drawbacks that suggest not combining O'Shaughnessy and Panicacci et al at all. To get voltage reference signals, the current output of the O'Shaughnessy D/A converter would have to be transformed into a voltage, or some voltage signal in Panicacci et al would have to be transformed into a current.

There are a variety of active and passive circuits that can perform such voltage-to-current or current-to-voltage conversions. The problem is that a Panicacci et al array with multiple instances of an O'Shaughnessy D/A converter – i.e. an array with more than two columns – the inter-instance A/D accuracy is limited by the matching of the voltage-to-current or current-to-voltage circuitry rather than by O'Shaughnessy's

elaborate and expensive calibration circuitry. If the former is poorly matched, the latter goes to waste.

Panicacci et al include calibration circuitry in Fig. 4B, but the circuitry is used to eliminate the offset voltage of the comparator, not to tune reference voltage generation. The reference voltage generation itself relies on a set of binary-scaled capacitors. These are not calibrated, which suggests that the fabrication process accuracy is sufficient for the application at hand.

The inter-instance matching limitation and the lack of reference generation calibration suggest that there is no motivation for combining O'Shaughnessy and Panicacci et al.

Moreover, as is clear from Panicacci et al Figs. 4A and 4B, there are lots of other circuit elements which are likely to be poorly matched – in fact, the usual suspects that drive the need for post-conversion processing – transistors in the APS cells, column bus length differences, sampling capacitors, holding capacitors, transmission gates, and amplification circuits, among others.

The improved performance of O'Shaughnessy's D/A converter – as measured in linearity of response – does not translate well when applied to Panicacci et al.

16 – Overall speed in Panicacci et al arises from parallel use of relatively slow A/D converters, whereas speed in O'Shaughnessy is essentially serial

Panicacci et al maintain throughput in a large array by using parallel instances of relatively slow A/D converters. Figs. 4A and 4B show a low-precision (8-bit) successive-approximation A/D converter. Panicacci et al could easily have proposed a fast 8-bit flash A/D converter, but did not, which suggests that compactness is more important than speed in the given circumstances.

Throughput in O'Shaughnessy is essentially serial. Switched-current D/A converters are inherently fast because transistor switching of currents and combination at a summing junction are fast. A drawback to the speed is that the circuits are not compact, particularly in O'Shaughnessy's D/A converter wherein the current sources and

calibrating circuitry are identical and exponential in number with resolution rather than binary scaled and linear in number with resolution.

O'Shaughnessy's calibration circuit seeks to improve on the decent matching of current sources to effectively eliminate differential and integral nonlinearity of the corresponding D/A converter. For the D/A converter of O'Shaughnessy Fig. 11, O'Shaughnessy cites on Column 18, lines 35-42, the following results:

> The DAC of FIG. 11 using an lux with a current source MOS transistor 1114X as described would have a DNL of 0.02 LSB. The INL for the DAC of FIG. 11 is the error resulting from the charge pump resolution for N stages. Assuming that this error is randomly distributed, the total expected error is the charge pump error multiplied by the square root of N plus DNL. A worst case INL error of 0.05 LSB is obtainable.

In other words, the DNL and INL are within the resolution limits of the converter.

These results are nice, but they come at a cost that makes O'Shaughnessy's invention ill-suited to the CMOS imaging system of Panicacci et al. O'Shaughnessy states in Column 6, lines 57-60:

> In addition, the invention provides improved performance for switched current DACs by significantly decreasing the mismatch error of unit current sources and ratio errors in bit weighted arrays.

This means that for N-bit D/A conversion, there are (2^N – 1) nominally identical current sources and (2^N – 1) charge pump circuits. For the 10-bit D/A converter of O'Shaughnessy Fig. 11, there would be 1023 current sources and 1023 charge pump circuits of Fig. 10. For a 12-bit version there would be 4095 of each, for a 14-bit version there would be 16383 of each, and for a 16-bit version there would be 65535 of each. In the charge pump circuit of Fig. 10 alone there are 20 explicit and implicit transistors, plus those of the bias circuit.

At low resolutions (8 or 10 bits), there are alternative fast A/D structures that have a cost which is exponential with resolution that might well be preferable to an A/D converter with O'Shaughnessy's exponential-cost D/A converter as an internal component, for instance, flash or half-flash A/D converters. At higher resolutions, O'Shaughnessy's invention is impractical.

Summary of Applicant discussion of 35 U.S.C. 103 rejections of Office Action B

With respect to 35 U.S.C. 103 rejection requirements, Applicant submits that:

- Office Action B fails to show suggestion or motivation for the combination of O'Shaughnessy and Panicacci et al.
- O'Shaughnessy and Panicacci et al do not show suggestion or motivation for combination with each other.
- The combination suggested by Office Action B fails to have a reasonable expectation of success.
- In the combination suggested by Office Action B, the individual parts no longer function for their original intended purpose.
- The combination suggested by Office Action B fails to have all the elements of any of the rejected claims.

Applicant therefore requests withdrawal of the rejections of Amendment A claims **2** and **7-11** under 35 U.S.C. 103(a) in view of O'Shaughnessy and Panicacci et al.

Conclusion

For all the above reasons, the Applicant submits that the specification and the claims are now in proper form, and that the claims are all patentable over the prior art. Therefore, the Applicant submits that this application is now in condition for allowance, which action is respectfully solicited.

Conditional Request for Constructive Assistance

The Applicant has amended the specification and claims of this application so that they are proper, definite, and define novel structure which is also unobvious. If, for any reason this application is not believed to be in full condition for allowance, the Applicant, an independent inventor and pro se filer, respectfully requests the constructive assistance and suggestions of the Examiner pursuant to M.P.E.P SS 2173.02 and SS 707.07(j) in order that the undersigned can place this application in allowable condition as soon as possible and without the need for further proceedings.

Very Respectfully,

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Certificate of Mailing: I hereby certify that this correspondence, and attachments, if any, will be deposited with the United States Postal Service by Overnight Mail, postage prepaid, in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date below.

October 1, 2005 Charles Douglas Murphy

Charles Douglas Murphy, Applicant